

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
6 October 2005 (06.10.2005)

PCT

(10) International Publication Number
WO 2005/093575 A1

(51) International Patent Classification⁷: **G06F 11/26**

(21) International Application Number:
PCT/KR2005/000668

(22) International Filing Date: 9 March 2005 (09.03.2005)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:
10-2004-0017476 9 March 2004 (09.03.2004) KR
10-2004-0019066 16 March 2004 (16.03.2004) KR
10-2004-0055329 12 July 2004 (12.07.2004) KR
10-2004-0093309 8 November 2004 (08.11.2004) KR
10-2005-0007330 24 January 2005 (24.01.2005) KR

(71) Applicant and

(72) Inventor: YANG, Seiyang [KR/KR]; 107-704 Sunkyung-Apt., Bugok-dong, Geumjung-gu, Pusan 609-320 (KR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

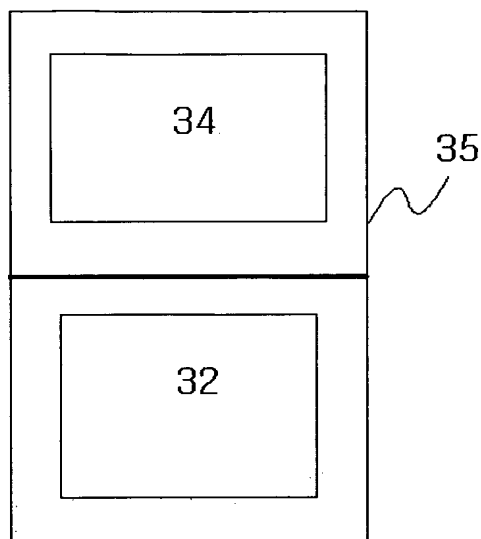
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DYNAMIC-VERIFICATION-BASED VERIFICATION APPARATUS ACHIEVING HIGH VERIFICATION PERFORMANCE AND VERIFICATION EFFICIENCY AND THE VERIFICATION METHODOLOGY USING THE SAME



(57) Abstract: The present invention relates to a simulation-based verification apparatus and a verification method, which enhance the simulation performance and efficiency greatly, for verifying a digital system containing at least million gates. Also, the present invention relates to a simulation-based verification apparatus and a verification method used together with formal verification, simulation acceleration, hardware emulation, and prototyping to achieve the high verification performance and efficiency for verifying a digital system containing at least million gates.

WO 2005/093575 A1